UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
ADDRESS: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,394	01/16/2002	Michael Fliesler	F0466	6188

7590 01/24/2003

Himanshu S. Amin
Amin & Turocy, LLP
24th Floor, National City Center
1900 E. 9th Street
Cleveland, OH 44114

EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	7

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
10/050,394	FLIESLER ET AL
Examiner	**Art Unit**
Thomas L Dickey	2826

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *9-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s): *2*
4)☐ Interview Summary (PTO-413) Paper No(s). ___
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II. claims 1-8 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement. the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

2. The oath/declaration filed on 01/16/02 is acceptable.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore. the power supply clamp diode of claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

4. Applicants have made no claim for priority.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 02/26/02 has been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In line 2, the term "2V" is undefined. For examining purposes it will be assumed applicant meant to say "Vcc + Vss [not 2V] <... where Vcc is the supply voltage and Vss is the floating supply voltage...."

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-4 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART.

The admitted prior art discloses a system for protecting an integrated circuit from electrostatic discharge with a core region (DIE CORE); a pad (PAD) electrically coupled to the core region (DIE CORE) through an input device (THE INVERTER CONSISTING OF PMOS AND NMOS TRANSISTORS 16 AND 18), the input device having at least one CMOS device with a gate oxide layer; and at least one protection diode 12, 14 operable to provide a discharge path for electrostatic discharge due to a high voltage being applied to the pad, the at least one diode comprising a first diode 12 and a second diode 14 forming an input protection circuit adapted to protect the input device, and the input device being a CMOS inverter formed from the aforesaid PMOS an NMOS transistors. Note figure 1 of the instant application. The admitted prior art does not disclose that the at least one protection diode has a reverse breakdown voltage less than the breakdown voltage of the gate oxide layer, nor that the reverse breakdown voltage of the at least one diode is greater than the supply voltage Vcc, or greater Vcc + Vss, and less than the breakdown voltage of the gate oxide layer.

However, one having skill in the art would have understood that Bvr must be less than Bvox because the ESD circuit is triggered by voltage spikes greater than Bvr. If the gate oxide were to break down before the ESD triggered, the ESD would never trigger, because the harmful voltage spike would be discharged through the gate oxide, and down the drain of the MOSFET to ground. One having skill in the art would understand that such an event would also destroy the device the ESD is meant to protect. One having skill in the art would also have understood that if Bvr were less than Vcc the ESD device would trigger while the input was at zero volts so that the ESD would interfere with ordinary operation of the device it is intended to protect. One having skill in the art would further understand that in a CMOS circuit with a floating supply voltage Vss, the normal lower limit for input voltage is below zero volts and is in fact –Vss. For this reason one having skill in the art would understand that Bvr must be greater than the normal swing of voltage between Vcc and the input voltage, said voltage swing being Vcc minus (-Vss), in other words, Vcc + Vss. Therefore, it would have been obvious to a person having skill in the art to set the Bvr of the at least one diode of the admitted prior to the claimed range of values in order to assure proper operation of the input device while still protecting the input device from electrostatic events.

B. Claims 5,6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of ITO ET AL. (5,416,351).

The admitted prior art discloses a system for protecting an integrated circuit from electrostatic discharge with a core region (DIE CORE): a pad (PAD) electrically coupled to the core region (DIE CORE) through an input device (THE INVERTER CONSISTING OF PMOS AND NMOS TRANSISTORS 16 AND 18). the input device having at least one CMOS device with a gate oxide layer: and at least one protection diode 12. 14 operable to provide a discharge path for electrostatic discharge due to a high voltage being applied to the pad. Note figure 1 of the instant application. The admitted prior art does not disclose that the at least one protection diode has a reverse breakdown voltage less than the breakdown voltage of the gate oxide layer, nor that the at least one diode comprises a power supply clamp diode. the at least one diode comprising a heavily doped N++ region and a heavily doped P++ region. nor that the core region comprises a flash memory device.

However. Ito et al. discloses a system for protecting an integrated circuit from electrostatic discharge with at least one diode comprising a power supply clamp diode. the at least one diode comprising a heavily doped N region 202 and a heavily doped P region (PBASE). and a core region comprising a flash memory device. Note figure 27A and column 22 line 65 of Ito et al. Further. one having skill in the art would have understood that Bvr must be less than Bvox because the ESD circuit is triggered by voltage spikes greater than Bvr. If the gate oxide were to break down before the ESD triggered. the ESD would never trigger. because the harmful voltage

spike would be discharged through the gate oxide, and down the drain of the MOSFET to ground. One having skill in the art would understand that such an event would also destroy the device the ESD is meant to protect. Therefore, it would have been obvious to a person having skill in the art to augment the admitted prior art's system for protecting an integrated circuit from electrostatic discharge with the at least one diode comprising a power supply clamp diode, the at least one diode comprising a heavily doped N region and a heavily doped P region and core region comprising a flash memory device such as taught by Ito et al. in order to provide a compact ESD protection device (the clamp diode utilizing heavily doped "Zener" diodes being capable of shunting more current in a smaller space than an ordinary diode, as Ito et al. point out) to thus provide better ESD protection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
01/2003